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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/500,254	02/08/2000	Hans Jurgen Mattausch	4853-000001	2313

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ALSTON & BIRD LLP
BANK OF AMERICA PLAZA
101 SOUTH TRYON STREET, SUITE 4000
CHARLOTTE, NC 28280-4000

EXAMINER
PORTKA, GARY J

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 07/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/500,254	Mattausch
Examiner	**Art Unit**
Gary J. Portka	2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 6, 2002* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-5* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *9, 10*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claim 1 has been amended by Applicant. Claims 1-5 are pending.

Information Disclosure Statement

2. The information disclosures submitted January 23, 2002 and May 13, 2002 (paper nos. 9 and 10) were considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 3/1 are rejected under 35 U.S.C. 102(e) as anticipated by Hubis, U.S. Patent 6,321,298 B1 (hereinafter "Hubis") or, in the alternative, under 35 U.S.C. 103(a) as obvious over

Hubis in view of Gujral et al., U.S. Patent 6,223,260 B1 (hereinafter "Gujral"), or alternatively over Hubis in view of Hamaguchi et al., U.S. Patent 6,021,472 (hereinafter "Hamaguchi").

6. As to claim 1, Hubis discloses the recited shared memory comprising: plurality of memories (202, Figure 3) accessible from a copybus side and a user side (host), at least one copybus (backend bus 110, Figure 3), the shared memory adapted to copy contents of one of the memories which has been changed by writing from the user side, to other memories through the copybus (see Abstract, column 2 lines 6-15). Hubis may be seen as having the recited ports connected respectively to user and copybus sides, and thus as a true multi-port memory as recited, since as shown in Figures 1 and 3, the controllers 104x may be considered a part of the memories, and the controllers are shown to have separate interfaces to the host side and the backend bus side.

Alternatively, it might be argued that the controllers are not a part of the memories, and thus that Hubis does not disclose that the memories are true multiport having at least one port connected to each of the user side and the copybus side. However, the use of multiport caches in such a configuration is well known in the art, and is taught by Gujral (see Figure 1, column 2 lines 46-50 and column 4 lines 32-35), and by Hamaguchi (see Figures 1 and 2). Note in particular the cache memories 11 and 16 of Hamaguchi are depicted as comprising controllers, and separate interfaces at the top and bottom of Figure 2. The caches of Gujral and Hamaguchi are true multiport as recited since they have independent ports allowing concurrent internal accesses. An artisan would have been familiar with the well known advantages of improved performance of a multiport cache resulting from reduced contention and higher degree of parallel processing, and thus would have recognized the

benefits of making the memories of Hubis multiport with at least one port connected to each of user and copybus sides. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use multiport memories having at least one port connected to each of the user side and the copybus side, because this was taught by Gujral and Hamaguchi, and was a well known means of improving performance due to increased degree of parallel processing.

7. As to claim 3/1, Hubis discloses the memories are formed by an integrated circuit technique (see column 3 lines 15-20, where semiconductor RAM is considered as formed by an integrated circuit technique).

8. Claims 2, 3/2, and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis in view of Gujral, and further in view of Hirose, JP Patent 61-3450 (A) (hereinafter "Hirose"), or alternatively over Hubis in view of Hamaguchi, and further in view of Hirose.

9. As to claims 2, 3/2, and 5, neither Hubis, Gujral, nor Hamaguchi disclose copying optically. However, the technique was well known in the art and was taught by Hirose. The device of Hirose is taught to improve signal transmission speed in a shared memory, and clearly invokes the trend of reducing cost and improving performance by increasing integration as compared to the other references. The device is formed by a three dimensional integrated circuit technique. Thus it would have been obvious to one of ordinary skill in the art to copy optically with a three dimensional integrated circuit device, because such a device and method was previously taught by Hirose as improving performance.

10. As to claim 4, while Hirose teaches a three dimensional integrated device, an artisan would have known that older two dimensional devices were still applicable, and would have desired such a device for the purposes of reducing cost, or for compatibility with existing manufacturing facilities and/or interfacing circuits. Thus it would have been obvious to use a two dimensional integrated circuit technique, because this is well known as a cheaper manufacturing alternative, and may improve compatibility requirements.

Response to Arguments

11. Applicant's arguments filed June 6, 2002 have been fully considered but they are not persuasive.

Applicants argue that the cited art does not teach a true multiport memory that allows independent ports internal concurrent accesses. Examiner does not agree; the multiport memories of Gujral and Hamaguchi have independent ports that allow internal concurrent accesses to the memory. The limitation "internal" includes the circuits shown in Gujral Figure 9 or Hamaguchi Figure 2; that is, internal concurrent accesses are not construed as exclusively internal to the data arrays therein, but as internal to the entire circuit that makes up the described memory as shown in the figures cited. Note that Gujral Figure 9 is a detailed diagram of one of the memories HL 14 shown in Figure 1; likewise Hamaguchi Figure 2 is a detailed diagram of one of the caches 11 or 16 of Figure 1. The arguments in regard to this that also point out that a true multiport memory has higher bandwidth than a pseudo multiport memory, but the claim language does not support this argument. It is further noted that Applicants own specification appears to acknowledge that such

multiport memories were well known in the art (page 7, "Each multi-port memory 11-1, 11-2,...., 11-p may be constructed by any known multi-port memory.").

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication from the examiner should be directed to Gary J. Portka at telephone number (703) 305-4033. The examiner can normally be reached on weekdays from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo, can be reached at (703) 308-4908.

Any response to this final action should be mailed to (or faxed as provided below):

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Fourth Floor (Receptionist).

The fax phone number for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final communications)

(703) 746-7239 (Official communications)

(703) 746-7240 (Status inquiries, draft communications)

Any inquiry of a general nature relating to this application or proceeding should be directed to the Group receptionist, whose telephone number is (703) 305-3900.

Gary J. Portka
Patent Examiner
July 17, 2002